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Physical planning of on-chip interconnect architectures

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Dept. of Comput. Sci. & Eng., Univ. of California, La Jolla, CA, USA

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Abstract
Interconnect architecture plays an important role in determining the throughput of meshe structures. We assume a mesh structure with uniform communication demand for commu commodity flow (MCF) model is proposed to find the throughput for several different routi experimental results reveal several trends: 1. The throughput is limited by the capacity of **column** in the mesh, simply enlarging the congested channel cannot produce better throu shape provides around 30% throughput improvement over a square chip of equal area. 2 allows 17% throughput improvement over 90-degree mesh and a 90-degree and 45-degr provides 30% throughput improvement. 3. To achieve maximum throughput on a mixed M diagonal **interconnect** architecture, the best ratio of the capacity for diagonal routing laye for Manhattan routing layers is 5.6. 4. Incorporating a simplified via model, interleaving di and Manhattan routing layer is the best way to organize the wiring directions on different l

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Non-controlled Indexing
congested channel diagonal **interconnect** architecture flexible chip shape me meshed communication structures mixed Manhattan **interconnect** architecture commodity flow model on-chip **interconnect** architectures physical planning via model
Author Keywords
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